Shri Shankaracharya Technical Campus,

Shri Shankaracharya Group of Institutions

(An Autonomous Institute affiliated to CSVTU, Bhilai)

SCHEME OF TEACHING AND EXAMINATION

Courses of Study and Scheme of Examination of M. Tech

1st Semester M.Tech. Electronics &Telecommunication (Communication)

S. No.	Boardof Study	Subject Code	Subject	Periods per week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
							Theory/Practical				
				L	T	P	ESE	CT	TA		
1.	Electronics & Telecom	ET222101	Modern Digital Communication Techniques	3	1	-	100	20	20	140	4
2.	Electronics & Telecom	ET222102	Communication Hardware Design Using VH DL	3	1	-	100	20	20	140	4
3.	Electronics & Telecom	ET222103	High performance communication network	3	1	-	100	20	20	140	4
4.	Electronics & Telecom	ET222104	Microwave & Radar Engineering	3	1	-	100	20	20	140	4
5.	Electronics & Telecom	Refer Table I	Elective – I	3	1	-	100	20	20	140	4
6.	Electronics & Telecom	ET222191	VHDL Design Lab	-		3	75		75	150	2
7.	Electronics & Telecom	ET222192	Modern Digital Communication Techniques Lab	-		3	75		75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

Table I

Elective-I			
Sr.No.	**Board of Study**	**Subject Code**	**Subject**
1	Applied Mathematics	ET222121	Applied Mathematics for Electronics Engineer
2	Electronics & Telecom	ET222122	Satellite Communication
3	Electronics & Telecom	ET222123	Digital System Design

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L-Lecture T- Tutorial P-Practical

CT- Class Test TA- Teachers Assessment ESE- End Semester Exam

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semister M.Tech. Electronics &Telecommunication (Communication)

Subject Code :- ET222101	**Modern Digital Communication Techniques**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of **Digital Transmission Schemes** . The aim is to impart skills to students for **developing various Algorithms and advanced techniques** that can improve the perforformance of digital Communication .	On successful completion of the course, the student will be able to: **CO1:-**Outline the features of basics of digital Communication and its transmission Process. **CO2:-**learn various digital modulation techniques. **CO3:-**calculate various efficiency analysis parameters of digital Communication . **CO4**:-Understand various type of channels and its effect on signal transmission. **CO5:-**Learn the Various encoding and Decoding schemes in digital Communication.

UNIT-I:INTRODUCTION :

CO1

Functional Architecture Coded And Encoded Digital Communication System Architecture, Types of Networks And Services , Performance Criterion And Link Budgets.[5Hrs]

UNIT–II: DIGITAL MODULATIONS: **CO2**

PSD , DTA Pulse Stream, M-Ary Markov Source, Convolutionally Coded Modulation, Continuous Phase Modulation (CPM) , Scalar And Vector Communications Over Memory Less Channel , Scalar Receiver, BER Performance , Detection Criterion. [5Hrs]

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UNIT – III Coherent And Non-Coherent Communication With Waveforms: **CO3**

Optical Receiver In WGN, MF Receiver, Matrix Generation, Colored GN, Whitening Approach ,In-phase And Quadrature Phase Modem, Non- Coherent Receivers, Random Phase Channel, Optimum And Suboptimum M-FSK, Performance Of Non- Coherent Receivers In Random Phase Channel, Optimum Receivers In RayleighAnd Rician Channels, M- Ary Symbol Error Probability. [5Hrs]

UNIT – IV Band Limited Channels: **CO4**

Optimum Pulse Shape Design, Optimum Demodulations Of Digital Signals In The Presence of ISI And AWGN Equalization Techniques, Diminishing And Detection –Q Modulation , QAM , QPSK, QBM, CPM , FSK, MSK.**[5Hrs]**

UNIT – V Coded digital communication: **CO5**

Architecture , Interfacing , Detailing, Synchronization , Block Coded Digital Communication System Performance , Types of Binary Block Codes , Shanon Channel Coding Theorem , Linear Block Codes, Conventional Coded Digital Communication System, Representation of Convolution Codes, Decoding Problems of Decreasing Errors, Sequencing And Threshold Decoding.[5Hrs]

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Digital Communication Techniques	M.K. Simon, S.M. Hinedi, W.C. Lindsey	Second	Prentice Hall India, New Delhi, 1995
2	Digital Communications	Simon Haykin	Eight	John Wiley and sons 1998

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Advanced Electronic Communication Systems	Wayne Tomasi	Fourth	Oxford University Press,1998
2	Modern Digital and Analog Communication Systems	B.P. Lathi	Third	Oxford University Press ,1998

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M.Tech. Electronics &Telecommunication (Communication)

Subject Code :- ET222102	COMMUNICATION HARDWARE DESIGN USING VHDL	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students able to acquire knowledge on Hardware Description Languages, Programmable logic devices and FPGAs, on the basic of VHDL languages learn the design and realization of combinational & sequential digital circuits.. The aim is to impart skills to students for design and simulation of different communication circuits..	On successful completion of the course, the student will be able to: **CO1:-**design digital circuit using HDL and explain the architectures of Programmable logic devices and FPGAs **CO2:-**model digital systems in HDL at different levels of abstraction. **CO3**understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements. **CO4:-**Design finite state machines for various applications **CO5:-**Analyse& simulate various modulator and demodulator circuit configurations and their applications

UNIT I DESIGN CONCEPT **CO1**

Digital Hardware, Design Process, Design of Digital Hardware, Programmable Logic devices(PLA, PAL, CPLD, FPGA) **[5Hrs]**

UNIT – II HARWARE MODELING **CO2**

Introduction, Hardware Modeling Languages, Abstract Models, compilation and behavioral optimization, perspectives.**[5Hrs]**

UNIT – III DIGITAL CIRCUIT DESIGN **CO3**

Multiplexes, Decoders, Encoders, Code Converters, Arithmetic Comparison Circuit, VHDL for Combinational Circuits: Assignment Statement, Selected Signal Assignment, Conditional Signal Assignment, Generate Statement, Concurrent and Sequential Statement assignment statement, Process Statement, Case Statement. FlipFlops, Registers and Counters. **[5Hrs]**

UNIT – IV: SEQUENTIAL CIRCUIT DESIGN: **CO4**

Basic Design Steps, State assignment problem, Mealy State Model, Design of FSM, Asynchronous Behavior, Analysis of Asynchronous Circuits, State Reduction, State Assignment Problem.**[5Hrs]**

UNIT – V:Simulation Of Communication Circuits **CO5**

Design of FSK Modulator , Simulation of FSK Modulator , Design of FSK Demodulator , Simulation of FSK Demodulator, Design and Simulation of Filters. **[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Fundamentals of Digital Logic with VHDL Design	Brown Vranesic	Second	TMH Publication
2	Synthesis and Optimization of Digital Circuits	Giovanni De Micheli	Third	TMH Publication
3	Analog Integrated Circuit Design	D. A. Johns and K. Martin	Second	Wiley

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Circuit Design with VHDL	Pedroni	Second	PHI Publication
2	VHDL Primer	Bhaskar	Third	PHI Publication

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M.Tech. Electronics &Telecommunication (Communication)

Subject Code :- ET222103	**High Performance Communication Network**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of **High performance communication network** . The aim is to impart skills to students for developing and hosting computer network establishment.	On successful completion of the course, the student will be able to: **CO1:-**Outline the features of basics of computer network. **CO2:-** Design structure of packet switched network.. **CO3:-** Design structure of internet and TCP/IP networks.. **CO4:-** learn the structure of atm and wireless networks. **CO5:-**Learn the structure of optical network and switching.

UNIT- I: Basics Of Networks : **CO1**

Telephone , computer, Cable television and Wireless networks, working principles, Digitization: Service Integration network services and layered architecture traffic characterization and QOS, network services: network elements and network mechanisms **[5Hrs]**

UNIT–II : Packet Switched Networks : **CO2**

0SI and IP Model, Different Layers, Performance issues of flow control protocols Packet Switching :Optimum packet size, Routing Strategies LAN Protocols; Ethernet (IEEE 802.3); token ring (l EEE 802.5),FDDI, DQDB, SMDS ,Frame relay**[5Hrs]**

UNIT – III: Internet And TCP/IP Networks : **CO3**

Overview; Internet protocol; TCP and VDP; performance of TCP/IP networks :SONET; DWDM, Fiber to home, DSL Intelligent networks. CATV.**[5Hrs]**

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UNIT – IV: ATM and Wireless Networks : **CO4**

Main features-addressing, signaling and routing: ATM header structure -adaptation layer, management and control; B-ISDN, interworking with ATM, Wireless networks: Spread spectrum LANs, IR LANs **[5Hrs]**

UNIT – V :Optical Networks and Switching : **CO5**

Optical links- WDM systems. Optical LAN's, optical paths and networks; TDS and SDS: Distributed, shared input and output buffers **[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	High Performance Communication Networks	Jean Warland and Pravin Varaiya	Second	Harcourt and Morgan Kauffman , London, 2000
2	Data and computer Communication	Willium Stalling	Eight	Pearson Prentice Hall

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Communication Networks	Leon Gracia, Widjaja	Second	Tata McGraw -Hill, New Delhi, 2000
2	ATM Networks	Sumit Kasera , Pankaj Sethi	Fourth	Tata McGraw-Hill, New Delhi, 2000

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M.Tech. Electronics & Telecommunication (Communication)

Subject Code :- ET222104	**Microwave & Radar Engineering**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of **Secure Communication**. The subject aims to provide the student with: 1. An understanding of microwave components, devices, tubes and network analysis. 2. An ability to perform microwave measurements. 3. An understanding of MTI RADARs and its applications. 4. An understanding of radio navigation and Microwave landing system.	On successful completion of the course, the student will be able to: **CO1:-** Understand microwave components such as Tee Junction, Directional Couplers and Signal generators. **CO2:-** Understand the theory of microwave cavity and various microwave measurement techniques. **CO3:-** Understand the need and working of Microwave devices and amplifiers. **CO4:-** Gain in depth knowledge about the MTI radar,its operation and Radio Navigation techniques. **CO5:-** Become familiar with aircraft homing system and microwave landing system.

UNIT- I: Industrial Microwaves & Component: **CO1**

Microwave Waveguide Components: Attenuators, phase shifters, matched loads, detectors and mounts, slotted-sections, E-plane tee, H-plane tee, hybrid tees, directional douplers, tuners, circulators and isolators; Signal generators: Fixed frequency,sweep frequency and synthesized frequency oscillators; Microwave in process control instrumentation **[5Hrs]**

UNIT–II: Microwave Measurement Techniques: **CO2**

Noise sources and noise meters used in microwave measurements; Frequency meters and VSWR meters; Measurements of frequency, attenuation,VSWR and impedance; Cavity measurements: Q -factor, bandwidth; Cavity and Waveguide methods;Measurements of power Calorimetric and Microwave bridges; Principles of

time domain and frequency domain reflectometry, spectrum analyser and network analyser; Measurement of Scattering parameters of passive and active devices **[5Hrs]**

UNIT – III: Microwave Devices and Amplifiers: **CO3**

Microwave Transistor; Microwave Tunnel Diode; Varacter Diode; Schottky Diode; MESFET: Principle of operation, equivalent circuit, cut off frequency, power frequency limitations; Charge Coupled Devices (CCD); Transferred Electron Devices: Gunn Diode, LSA Diode, modes of operation, Microwave Generation and Amplification; Avalanche Effect Devices: Read diode,carrier current and external current; IMPATT diodes. Klystron: Velocity modulation process, bunching process, output power and beam loadin g; Reflex Klystron: power output and efficiency; Traveling Wave Tubes; Magnetron. **[5Hrs]**

UNIT – IV: MTI Radar, Transmitter and Receiver: **CO4**

Oscillator amplifier, mixer, displays, duplexer, matched filter, receiver, correlation, detection, constant falls alarm rate, receiver, protector, selectivity, time control., Introduction , Operation of MTI Radar , MTI Receiver With Delay Line , Cnceler Range Gated, Doppler Filter, Digital Signal Processing, MTI For A Moving Platform , Limitations of MTI Platform. **[5Hrs]**

UNIT – V: Aircraft Homing System And Instrument Loading System: **CO5**

Introduction, Switched cardiod homing system, four course radio range, omnidirectional ranges, tactical air navigation, instrument landing aids, ground controlled approach, radio altimeter, microwave landing system, advantages of MLS. **[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Microwave Devices & Circuits	Liao, Samuel Y.	Second	PHI
2	Introduction to radar system	MERRICC, I-SKOC, NIK	Eight	TMH

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Passive Rf & Microwave Integrated Circuits	Maloratsky ,Leo G	Second	Elsevier
2	Recent Advances In Microwaves & Lightwaves	E.K. Sharma	Fourth	New Age

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (Communication)

Subject Code :- ET222123	**Digital System Design**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of **Digital System Design**. The aim is to impart skills to students for developing and designProcessor, Computer Arithmetic and the Arithmetic Unit, Memory System.	On successful completion of the course, the student will be able to: **CO1:**-Able to learn the General Purpose Machine, Languages and Digital Logic. **CO2:-** Design structure of Processor. **CO3:**-Able to understand and Design structure of Computer Arithmetic and the Arithmetic Unit. **CO4:**-learn about Memory System Design. **CO5:**-Able to understand Digital system Input and Output.

UNIT- I :The General Purpose Machine, Languages and Digital Logic: **CO1**

The General Purpose Machine, User's View, The Machine/Assembly Language Programmer's View The Computer Architect's View, The Computer System Logic Designer's View, Classification of Computers and Their Instructions, Computer Instruction Sets, Informal Description of the Simple RISE Computer, SRC , Formal Description of SRC Using Register Transfer Notation, RTN , Describing Addressing Modes with RTN ,Register Transfers and Logic Circuits: From Behavior to Hardware. **[5Hrs]**

UNIT–II: Processor Design: **CO2**

The Design Process, AI-Bus Micro architecture for the SRC, Data Path Implementation, Logic Design for the I-Bus SRC, The Control Unit, The 2- and 3·Bus Processor Designs, The Machine Reset, Machine Exceptions, Pipelining, Instruction-Level Parallelism, Microprogramming. **[5Hrs]**

UNIT – III :Computer Arithmetic and the Arithmetic Unit: **CO3**

Number Systems and Radix Conversion, Fixed-Point Arithmetic, Seminumeric Aspects of ALUDesign, Floating-Point Arithmetic. **[5Hrs]**

UNIT – IV: Memory System Design: **CO4**

The Components of the Memory System, RAM Structure, The Logic Designer's Perspective, MemoryBoards and Modules, Two-Level Memory Hierarchy, The CacheVirtual Memory, The Memory Subsystem in the Computer**. [5Hrs]**

UNIT – V :Input and Output: **CO5**

The I/O Subsystem, Programmed I/O, I/O Interrupts, Direct Memory Access (DMA) ,I/O Data Format Change and Error Control. **[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Computer Systems Design and Architecture	Vincent P. Heuring& H. Jordan	Second	Pearson Education
2	Computer organization & Architecture	Stallings	Tenth	Pearson Education

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Digital System Design & Microprocessors	Hayes, John P	Second	Tata McGraw -Hill, New Delhi, 2000
2	Digital System (Principles & Applications)	R.J. tocci	Tenth	P.H.I.

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (Communication)

Subject Code :- ET222191	VHDL Design Lab	**L = 0**	**T = 0**	**P = 2**	**Credits = 2**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**Lab Periods**
	75	**00**	**75**	**150**	**10**

Course Objective	**Course Outcomes**
The objective is to make the students able to acquire knowledge on Hardware Description Languages, Programmable logic devices and FPGAs, on the basic of VHDL languages learn the design and realization of combinational & sequential digital circuits.. The aim is to impart skills to students for design and simulation of different communication circuits..	On successful completion of the course, the student will be able to: **CO1:-**design digital circuit using HDL and explain the architectures of Programmable logic devices and FPGAs **CO2:-**model digital systems in HDL at different levels of abstraction. **CO3**understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements. **CO4:-**Design finite state machines for various applications **CO5:-**Analyse& simulate various modulator and demodulator circuit configurations and their applications

List of Experiments

1) To design and simulate the basic gates CO1
2) Designing of the combinational blocks a) Mux b) Encoders c) Decoders CO2
3) Designing and simulation of Code converters CO3
4) Designing, simulation and implementation 9-bit parity generator/checker CO4
5) Designing, simulation and implementation Flip-Flops CO1
6) Designing and simulation of Registers CO5
7) Designing and simulation of Counters CO2
8) FSM modeling (Design Sequence Detector “101”) CO4
9) Designing, simulation and implementation of ROM CO3
10) Designing, simulation and implementation of RAM CO5

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List of Equipments/Machine Required:

1) Computer System with Pentium 4 processor, 256MB Ram 2) EDA tools: 1) FPGA implementation kit 2) CPLD implementation kit 3) Xilinx project nevigator 5.2 4) Active HDL 6.2 5) Modelsim

2) Recommended Books:

1) Fundamentals of Digital Logic with VHDL Design: Brown Vranesic, TMH Publication.

2) Circuit Design with VHDL Prdroni PHI Publication

3) VHDL Primer Bhaskar PHI Publication

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (Communication)

Subject Code :- ET222192	Modern Digital Communication Techniques Lab	**L = 0**	**T = 0**	**P = 2**	**Credits = 2**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**Lab Periods**
	75	**00**	**75**	**150**	**10**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of **Digital Transmission Schemes** . The aim is to impart skills to students for **developing various Algorithms and advanced techniques** that can improve the performance of digital Communication .	On successful completion of the course, the student will be able to: **CO1:-**Outline the features of basics of digital Communication and its transmission Process. **CO2:-**learn various digital modulation techniques. **CO3:-**calculate various efficiency analysis parameters of digital Communication . **CO4**:-Understand various type of channels and its effect on signal transmission. **CO5:-**Learn the Various encoding and Decoding schemes in digital Communication.

List of Experiments

i.	To generate various signals used in digital communications	CO1
ii.	To find correlation autocorrelation between various signals	CO2
iii.	To find convolution of signals and simulate response of LTI system	CO3
iv.	To write different algorithms of FFT	CO4
v.	To design IIR and FIR digital filters	CO5
vi.	To use raised cosine filters for pulse shaping	CO2
vii.	To source code using DPCM, Huffman etc.	CO3
viii.	To channel code and verify Shannon's channel capacity	CO3
ix.	To modulate signals using ASK, PSK, MSK etc in presence of AWGN	CO4
x.	To study and simulate the effects of equalization	CO2

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Chairman (AC)	Chairman (BoS)	Date of Release	Version	

List of Equipments/Machine Required:

i. Mat lab 7.0
ii. Computer System (PIV with 256 MB Ram)
iii. CDMA trainer
iv. GSM trainer
v. Spectrum Analyzer

Recommended Books:

1. M.K. Simon, S.M. Hinedi and W.C. Lindsey, " Digital Communication Techniques": Signaling and detection, Prentice Hall India, New Delhi, 1995.
2. Simon Haykin, " Digital Communications" , John Wiley and sons , 1998.